Remarks

Claims 2, 4-5 and 10-14 are pending in the application, of which claims 2 and 11 are currently amended. New claims 15-19 are also added for consideration, and are fully supported by the specification as originally filed. Reconsideration and allowance of the application are respectfully requested.

The non-final Office Action dated September 13, 2007 lists the following rejections: claims 2, 4-5 and 10-14 stand rejected under 35 U.S.C. 102(b) over Osawa *et al.* (U.S. Patent No. 5,946,247); claim 4 stands rejected under 35 U.S.C. 102(b) over Osawa *et al.* or under 35 U.S.C. 103(a) in the alternative; claims 2, 4-5 and 10-14 stand rejected under 35 U.S.C. 102(e) over Satoh (U.S. Patent No. 6,477,672); and claims 2, 4-5 and 10-14 stand rejected under 35 U.S.C. 103(a) over Abramovici *et al.* ("Digital Systems Testing and Testable Design" pgs. 479-487) and Osawa *et al.* Applicant respectfully traverses these rejections.

With regard to the rejections of claims 2, 4-5 and 10-14 over Osawa and over Satoh, Applicant understands these references to exclusively teach the testing of memories, as opposed to the testing of logic as recited in Applicant's claims. Osawa and Satoh also do not appear to teach programmable test vector generation (admitted in the Office Action as to the Osawa reference in Section 3 relating to the 103(a) rejection over Abramovici and Osawa). For at least these reasons, the Osawa and Satoh references cannot be said to teach all aspects of Applicant's claims.

As Applicant has explained in paragraphs [0003] and [0004] of the present specification, and in the Appeal Brief filed May 29, 2007, the testing of logic can require a much larger and more complex set of test vectors than needed to test memories due to the different nature of the faults that are likely to occur. In the past, testing of logic has required either a large test vector memory external to the IC (increasing test system complexity and cost) or a test vector generator integrated directly into the IC (increasing chip design considerations and chip area, and hence chip costs). Testing of memories involves generating much smaller sets of simple test vectors, thus not presenting the problems solved by Applicant's claimed invention.

In addition, Applicant finds nothing in Osawa or Satoh to teach or suggest programming the programmable test vector generator to provide pseudo-random test

vectors and deterministic test vectors to the logic circuitry under test, to provide test vectors in real time to the logic circuitry under test, or to modify the test vectors based on the logic circuitry to be tested, as recited in the newly added claims.

Applicant therefore submits that neither Osawa nor Satoh disclose all the elements recited in the presented claims, and requests reconsideration and withdrawal of the rejections based on these references.

Claims 2, 4-5 and 10-14 stand rejected under 35 U.S.C. 103(a) over Abramovici and Osawa. As admitted in the Office Action, Osawa does not teach programmable test generation. Further, as discussed above, Osawa does not teach testing of such logic circuitry, and is directed only to testing memories. Abramovici relates to built-in self-testing of integrated circuits, and does not appear to disclose an external tester that includes a programmable test vector generator for testing logic circuitry. As such, any combination of Osawa and Abramovici, if proper, does not teach or suggest all the elements recited in Applicant's claims. Thus, a *prima facie* case of obviousness has not been stated.

In addition, Applicant finds nothing in Abramovici, or any proposed combination of Osawa and Abramovici, to teach or suggest programming the programmable test vector generator to provide pseudo-random test vectors and deterministic test vectors to the logic circuitry under test, to provide test vectors in real time to the logic circuitry under test, or to modify the test vectors based on the logic circuitry to be tested, as recited in the newly added claims.

For at least these reasons, Applicant requests reconsideration and withdrawal of the 103(a) rejection over Abramovici and Osawa.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063 (or the undersigned).

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